



Aldec and ASICSoft Partner to bring Free Quality Assertions Training to the Silicon Valley

Santa Clara, CA – July 12, 2011 Get ahead with free Seminar Training classes! Aldec and ASICSoft Partner to bring free quality Assertions Training to the Silicon Valley.

ASSERTIONS FOR HDL DESIGNERS

Thursday, August 18, 2011

The Biltmore Hotel

2151 Laurelwood Road
Santa Clara, CA 95054 [see map](#)

This half-day seminar is for hardware designers with practical knowledge of Verilog and/or VHDL. It prepares the student for practical usage of assertions in verification tools by explaining basic ideas, introducing key elements of assertions illustrated with simple examples and presenting complete design demonstrating various uses of assertions. Examples use SystemVerilog Assertions (SVA) and Property Specification Language (PSL) in parallel, giving students more options of further study. Presenter: Jarek Kaczynski, Aldec Research Engineer.

8:45am Registration
9:00am Session begins
11:30am Lunch (provided)
1:00pm Session ends

Seating is Limited. [Register today at aldec.com/events](http://aldec.com/events).

We invite you to share this free training information with your colleagues. For a printable event flyer, please click here [\[insert link\]](#). For more free educational tools, including webinars, technical papers, tutorials and more, please visit www.aldec.com.

About Aldec

Aldec Inc., headquartered in Henderson, Nevada, is an industry leader in Electronic Design Verification and offers a patented technology suite including: RTL Design, RTL Simulators, Hardware-Assisted Verification, Design Rule Checking, IP Cores, DO-254 Functional Verification and Military/Aerospace solutions. www.aldec.com

About ASICSoft

ASICSoft is an engineering services and product marketing company. Our mission is "Designs on Time". We partner with technical leaders in various aspects of their designs in order to assist them hit their design milestones on time.

www.asicsoft.com

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